

INT-CL (IEC): H01L029/786;G02F001/133
;G02F001/136 ;G09E009/33 ;B01L021/336

ABSTRACT:

PROBLEM TO BE SOLVED: To provide an active matrix type semiconductor device having no image irregularities.

SOLUTION: An analog switch 104 and a buffer 102 of a drive circuit are constituted and a plurality of analog switches and buffers that are constituted of TFTs with a small channel width are connected in parallel, and the traveling direction of the carriers of a plurality of TFTs and the scanning direction of a linear laser 409 that is used when crystallizing laser are inclined, thus capable of reducing the scattering of the characteristics of the analog switch and the buffer, of suppressing deterioration, and hence of achieving an active matrix type semiconductor device with less image irregularities.

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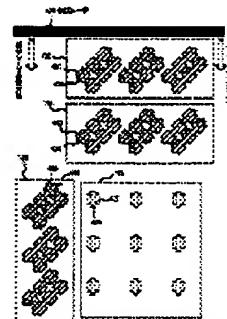
◎日本本邦税金 (C) (◎) 公開特許金額 (A) (◎) 特許公報登録料
特別平11-214700
(登録料: 特許公報登録料 6,650)

Subject	Address	PI	
HOLL	10700	HOLL	10700
GTZP	1133	GTZP	1133
	1133		500
GD97	9100	GD9P	9100
HOLL	21000	HOLL	21000

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教員評議會和市長評議會

33 電子の世界 半導体と元気



J.P. 11214700 A date is no good

DERWENT-ACC-NO: 2000-166871
DERWENT-WEEK: 200016
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TITLE: Thin-film transistor circuit for active matrix type semiconductor display device - has predetermined number of analog buffer circuits consisting of differential circuits and current mirror circuits, which are connected in parallel

PATENT-ASSIGNEE: SEMICONDUCTOR ENERGY LAB [SEME]

PRIORITY-DATA: 1998JP-0118092 (April 28, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
PAGES	MAIN-IPC	
JP 2000022462	January 21, 2000	N/A
019	H03F 003/68	

A

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO
JP2000022462A	APPL-DATE	
	N/A	1999JP-0048578
	February 25, 1999	

INT-CL (IPC): G02F001/136; H01L021/336 ; H01L027/08 ; H01L029/786 ; H03F003/45 ; H03F003/68

ABSTRACTED-PUB-NO: JP2000022462A

BASIC-ABSTRACT: NOVELTY - Predetermined number of analog buffer circuits

(A1-An) consisting of differential circuits (B1-Bn) and current mirror circuits

(C1-C3), are connected in parallel. DETAILED DESCRIPTION - An INDEPENDENT

CLAIM is also included for an active matrix type semiconductor display device.

USE - For active matrix type semiconductor display device.

ADVANTAGE - Characteristic variation of analog buffer causing image

irregularity of semiconductor display device, can be suppressed.

High-resolution semiconductor display device can be offered. DESCRIPTION OF

DRAWING(S) - The figure shows the circuit component of the analog buffer

circuit. (A1-An) Analog buffer circuits; (B1-Bn) Differential circuits;

(C1-C3) Current mirror circuits.

CHOSEN-DRAWING: Dwg.1/14

TITLE-TERMS:

THIN FILM TRANSISTOR CIRCUIT ACTIVE MATRIX TYPE
SEMICONDUCTOR DISPLAY DEVICE

PREDETERMINED NUMBER ANALOGUE BUFFER CIRCUIT CONSIST
DIFFERENTIAL CIRCUIT

CURRENT MIRROR CIRCUIT CONNECT PARALLEL

DERWENT-CLASS: P81 U12 U14 U24

EPI-CODES: U12-B03A; U14-K01A2B; U14-K01A3; U24-G02A1;
U24-G02F2;

SECONDARY-ACC-NO:

Non-CPI Secondary Accession Numbers: N2000-125365

L Number	Hits	Search Text	DB	Time stamp
1	1979	analog same buffer same parallel	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/08/22 13:47
2	25849	analog same buffer same parallel samd (active adj matrix)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/08/22 13:47
3	12	analog same buffer same parallel same (active adj matrix)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2002/08/22 13:48

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2020-2021 School Year - Grade 5 Math - Unit 1

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 Drafts

Digitized by srujanika@gmail.com

Active

11: (1979) analog same but

12: (25849) analog same but

2 E2. (E5549) analog same as

Category	Score	Details	Cost
High Priority	100	100% of the time, the system is performing as expected.	\$100
Medium Priority	50	50% of the time, the system is performing as expected.	\$50

U	I	Document ID	Issue Date	Pages	Title	Current CR	Current XRef R
1	Γ	US 20010045931 A1	20011129	19	Drive circuit of active matrix type display device	345/92	
2	Γ	US 20010024185 A1	20010927	17	Semiconductor display device	345/92	
3	Γ	US 20010011970 A1	20010609	17	DRIVE CIRCUIT OF ACTIVE MATRIX TYPE DISPLAY DEVICE	345/38	
4	Γ	US 6246387 B1	20010612	16	Semiconductor display device	345/92	345/205;
5	Γ	US 6232946 B1	20010515	29	Active matrix drive circuits	345/98	345/100
6	Γ	JP 11214700 A	19990806	12	SEMICONDUCTOR DISPLAY DEVICE		
7	Γ	JP 100000000000 A	19920312	7	LIQUID CRYSTAL DRIVING DEVICE		345/92
8	Γ	JP 2000194276 A	20000714	16	Active matrix type display device production procedure		
9	Γ	JP 2000155304 A	20000606	16	Active matrix type display device has each pair of		
10	Γ	JP 2000022462 A	20000121	19	Thin-film transistor circuit for active matrix type		
11	Γ	JP 10153860 A	19980609	16	Active matrix display device - has source drive circuit		
12	Γ	JP 08062637 A	20011122	19	Drive circuit for active matrix type display device -		
13							

INT-CL:[07], G09G003/36

US-CL-PUBLISHED: 345/92

US-CL-CURRENT: 345/92

REFERENCE-FIGURES: 1

ABSTRACT:

An active matrix semiconductor device is provided which is free of unevenness in image. The analog switch and buffer in a drive circuit are structured by a plurality of parallel -connected analog switches and buffers each formed by a TFT with a small channel width. The carrier moving direction of these TFTs are oblique relative to a scanning direction of a linear laser used for laser crystallization. By doing so, the analog switch and the buffer are decreased in characteristic variation with deterioration suppressed. Thus an active matrix semiconductor device is realized which is free of unevenness in image.

BRIEF SUMMARY:

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to semiconductor display devices with thin film transistors. More particularly, the

(s) United States

(s) Patent Application Publication (s) Pub. No.: US 2001/0024185 A1

(s) Pub. Date: Sep. 27, 2001

(s) SEMICONDUCTOR DISPLAY DEVICE

(s) Foreign Application Priority Data

(s) Inventor: Shigeaki Yamamoto (JP)

(s) Jan. 23, 2001 (JP) 15-02422

Correspondence Address:

Publication Classification

ATAGO PHAROSITY LTD.

(s) Int. Cl. 7 092 000 2006

10000 GAKUSHOCHO DRIVE

(s) 25000 346-72

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ABSTRACT

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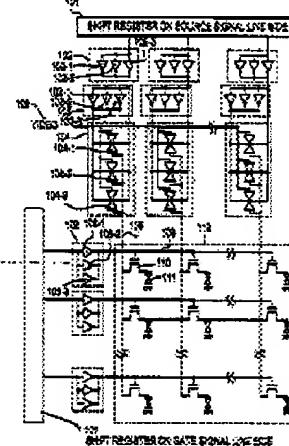
(s) An active matrix semiconductor device is provided which is free of unevenness in image. The analog switch and buffer in a drive circuit are structured by a plurality of parallel-connected analog switches and buffers each formed by a TFT with a small channel width. The carrier moving direction of these TFTs are oblique relative to a scanning direction of a linear laser used for laser crystallization. By doing so, the analog switch and the buffer are decreased in characteristic variation with deterioration suppressed. Thus an active matrix semiconductor device is realized which is free of unevenness in image.

(s) App. No.: 38997185

(s) Date: May 2, 2001

Related U.S. Application Data

(s) Division of application No. 09/229,443, filed on Nov. 20, 1999, and Pub. No. 6,200,387.



US 2001/0024185 A1 Doc 73

[0028] The present invention has been made in view of the above-described problems, and it is an object to provide an active matrix semiconductor display device which prevents unevenness in display caused due to unevenness in thin film transistors thereby realizing high image quality.

[0029] In the present invention, deterioration in image quality is prevented by preventing characteristic variation in the TFTs forming analog switches and buffers that are important in respect of having direct effects upon image quality for an active matrix semiconductor display device. More specifically, the TFTs forming an analog switch or buffer are divided into a plurality of parallel-connected TFTs having a smaller channel width.

[0030] Arrangement (patterning) is made such that the direction of the TFT active layers, i.e., carrier movement, is oblique relative to a direction of scanning a linear laser (laser beam) used to crystallize the semiconductor active layers during manufacturing the TFTs, or a direction perpendicular to the longitudinal direction.

[0031] It is known that if the TFT active layers are arranged oblique with respect to the linear laser beam scan direction as stated above, the individual TFTs have a characteristic decreased in

(s) United States

(s) Patent Application Publication (s) Pub. No.: US 2001/0024183 A1
(s) Date: Sep. 27, 2001

(s) SEMICONDUCTOR DISPLAY DEVICE

(s) Inventor: KAZUO TSURUMI, Applicant: (s)

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(s) Appl. No.: 09/999,203

(s) Date: May 2, 2001

Related U.S. Application Data

(s) Division of application No. 09/234,442, filed on Nov. 20, 1999, and PCT Int'l. Appl. No. PCT/JP00/04677.

(s) Foreign Application Priority Data

(s) Jan. 23, 1999 (JP) 10-024182

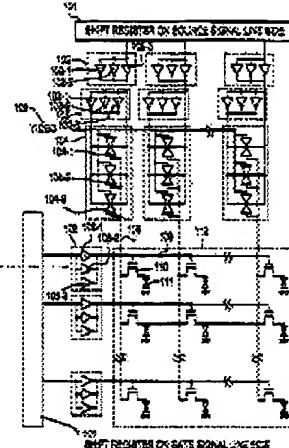
Publication Classification

(s) Int. Cl. 1600 350 340P

(s) Cl. 1600 340P

(s) ABSTRACT

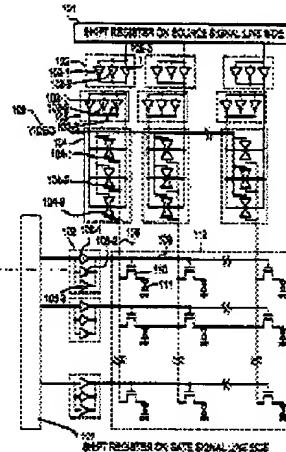
An active matrix semiconductor device is provided, which has a gate electrode, a source electrode and a drain electrode, a drain contact on a drain side of a drain electrode, a gate contact on a gate side of a gate electrode, and a source contact on a source side of a source electrode, the drain contact, the gate contact and the source contact being formed by a TFT with a small channel width. The source contact, drain contact and drain contact are formed by a source electrode, a drain electrode and a drain contact, respectively, by using a linear laser beam, and the gate contact is formed by a gate electrode, and the gate electrode is formed by a gate contact with a gate contact, respectively. Thus, an active matrix semiconductor device is formed with a fine of connection in size.



[0049] In the present embodiment, an active matrix liquid crystal display device is explained which has an analog switch directly connected to a source signal line, a last staged buffer for controlling the analog switch, and a buffer directly connected to a gate signal line, wherein each of them is divided into three connected in parallel.

[0050] Reference is now made to FIG. 1. 101 is a shift register provided on a side of source signal lines, 102 is a last staged buffer, 103 is a buffer for creating an inverted signal to a signal from the buffer 102, 104 is an analog switch, 105 is a video signal line, 106 is a source signal line, 107 is a shift register on a side of gate signal lines, 108 is a last staged buffer, 109 is a gate signal line (scan line), 110 is a pixel TFT, and 111 is a liquid crystal. Note that there are only shown, in FIG. 1, the analog switch 104 connected to the source signal line, last staged buffers 102 and 103, and the last staged buffer 108 directly connected to the gate signal line, with other circuits omitted for the sake of explanatory convenience. However, other circuits may be provided as required. The active matrix liquid crystal display device in this embodiment has pixels in number of 640 in horizontal.times.480 in vertical.times.RGB.

(s) United States
(s) Patent Application Publication
Yamazaki



L Number	Hits	Search Text	DB	Time stamp
15	15	"5335023"	USPAT; US-PPGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/22 18:39
16	7	"5335023" and buffer	USPAT; US-PPGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/22 18:39
17	2	"5335023" and buffer same parallel	USPAT; US-PPGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/22 18:40
18	2	"5335023" and buffer same parallel and active near5 matrix	USPAT; US-PPGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/22 18:40
-	1979	analog same buffer same parallel	USPAT; US-PPGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/22 13:47
-	25849	analog same buffer same parallel samd (active adj matrix)	USPAT; US-PPGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/22 13:47
-	12	analog same buffer same parallel same (active adj matrix)	USPAT; US-PPGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/22 18:38